Static Timing Analysis For Nanometer Designs A

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Long-Term Reliability of Nanometer VLSI Systems - Sheldon Tan 2019-09-12
This book provides readers with a detailed reference regarding two of the most important long-term reliability and aging effects on nanometer integrated systems, electromigrations (EM) for interconnect and biased temperature instability (BTI) for CMOS devices. The authors discuss in detail recent developments in the modeling, analysis and optimization of the reliability effects from EM and BTI induced failures at the circuit, architecture and system levels of abstraction. Readers will benefit from a focus on topics such as recently developed, physics-based EM modeling, EM modeling for multi-segment wires, new EM-aware power grid analysis, and system level EM-induced reliability optimization and management techniques. Reviews classic Electromigration (EM) models, as well as existing EM failure models and discusses the limitations of those models; Introduces a dynamic EM model to address transient stress evolution, in which wires are stressed under time-varying current flows, and the EM recovery effects. Also includes new, parameterized equivalent DC current based EM models to address the recovery and transient effects; Presents a cross-layer approach to transistor aging modeling, analysis and mitigation, spanning multiple abstraction levels; Equips readers for EM-induced dynamic reliability management and energy or lifetime optimization techniques, for many-core dark silicon microprocessors, embedded systems, lower power many-core processors and datacenters.
Nanometer Circuit Performance Analysis - Yu Cao 2002

Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava 2006-04-04
Covers the statistical analysis and optimization issues arising due to increased process variations in current technologies. Comprises a valuable reference for statistical analysis and optimization techniques in current and future VLSI design for CAD-Tool developers and for researchers interested in starting work in this very active area of research. Written by author who lead much research in this area who provide novel ideas and approaches to handle the addressed issues
The Art of Hardware Architecture - Mohit Arora 2011-10-09
This book highlights the complex issues, tasks and skills that must be mastered by an IP designer, in order to design an optimized and robust digital circuit to solve a problem. The techniques and methodologies described can serve as a bridge between specifications that are known to the designer and RTL code that is final outcome, reducing significantly the time it takes to convert initial ideas and concepts into right-first-time silicon. Coverage focuses on real problems rather than theoretical concepts, with an emphasis on design techniques across various aspects of chip-design.
Timing - Sachin Sapatnekar 2007-05-08
Statistical timing analysis is an area of growing importance in nanometer te- nologies, as the uncertainties associated with process and environmental var- tions increase, and this chapter has captured some of the major efforts in this area. This remains a very active field of research, and there is likely to be a great deal of new research to be found in conferences and journals after this book is published. In addition to the statistical analysis of combinational circuits, a good deal of work has been carried out in analyzing the effect of variations on clock skew. Although we will not treat this subject in this book, the reader is referred to [LNPS00, HN01, JH01, ABZ03a] for details. 7 TIMING ANALYSIS FOR SEQUENTIAL CIRCUITS 7.1 INTRODUCTION A general sequential circuit is a network of computational nodes (gates) and memory elements (registers). The computational nodes may be conceptualized as being clustered together in an acyclic network of gates that forms a c- binational logic circuit. A cyclic path in the direction of signal propagation 1 is permitted in the sequential circuit only if it contains at least one register . In general, it is possible to represent any sequential circuit in terms of the schematic shown in Figure 7.1, which has I inputs, O outputs and M registers. The registers outputs feed into the combinational logic which, in turn, feeds the register inputs. Thus, the combinational logic has I + M inputs and O + M outputs.
A Systemverilog Primer - J. Bhasker 2018-05-23
This book is an excellent resource to get up to speed on the application of the various features of SystemVerilog per IEEE 1800-2009. The explanations of each feature is provided with examples and guidelines, where appropriate. This book is well organized and full of concrete examples that illustrates well on how to use SystemVerilog. It is a must primer for anyone who is beginning to learn SystemVerilog.
Advances in VLSI, Communication, and Signal Processing - David Harvey 2020-10-14
This book comprises select peer-reviewed papers from the International Conference on VLSI, Communication and Signal processing (VCAS) 2019, held at Motilal Nehru National Institute of Technology (MNNIT) Allahabad, Prayagraj, India. The contents focus on latest research in different domains of electronics and communication engineering, in particular microelectronics and VLSI design, communication systems and networks, and signal and image processing. The book also discusses the emerging applications of novel tools and techniques in image, video and multimedia signal processing. This book will be useful to students, researchers and professionals working in the electronics and communication domain.
Using the Electric VLSI Design System - Steven M. Rubin 2009-02

Computational Science – ICCS 2020 - Valeria V. Krzhizhanovskaya 2020-06-19
The seven-volume set LNCS 12137, 12138, 12139, 12140, 12141, 12142, and 12143 constitutes the proceedings of the 20th International Conference on Computational Science, ICCS 2020, held in Amsterdam, The Netherlands, in June 2020.* The total of 101 papers and 248 workshop papers presented in this book set were carefully reviewed and selected from 719 submissions (230 submissions to the main track and 489 submissions to the workshops). The papers were organized in topical sections named: Part I: ICCS Main Track Part II: ICCS Main Track Part III: Advances in High-Performance Computational Earth Sciences: Applications and Frameworks; Agent-Based Simulations, Adaptive Algorithms and Solvers; Applications of Computational Methods in Artificial Intelligence and Machine Learning; Biomedical and Bioinformatics Challenges for Computer Science Part IV: Classifier Learning from Difficult Data; Complex Social Systems through the Lens of Computational Science; Computational Health; Computational Methods for Emerging Problems in (Dis-)Information Analysis Part V: Computational Optimization, Modelling and Simulation; Computational Science in IoT and Smart Systems; Computer Graphics, Image Processing and Artificial Intelligence Part VI: Data Driven Computational Sciences; Machine Learning and Data Assimilation for Dynamical Systems; Meshfree Methods in Computational Sciences; Multiscale Modelling and Simulation; Quantum Computing Workshop Part VII: Simulations of Flow and Transport: Modeling, Algorithms and Computation; Smart Systems: Bringing Together Computer Vision, Sensor Networks and Machine Learning; Software Engineering for Computational Science; Solving Problems with Uncertainties;

Teaching Computational Science; UNcErtainty QUantIficatiOn for ComputationAl modeLs *The conference was canceled due to the COVID-19 pandemic.

The Art of Timing Closure - Khosrow Golshan 2020-08-03

The Art of Timing Closure is written using a hands-on approach to describe advanced concepts and techniques using Multi-Mode Multi-Corner (MMMC) for an advanced ASIC design implementation. It focuses on the physical design, Static Timing Analysis (STA), formal and physical verification. The scripts in this book are based on Cadence® Encounter SystemTM. However, if the reader uses a different EDA tool, that tool's commands are similar to those shown in this book. The topics covered are as follows: Data Structures Multi-Mode Multi-Corner Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth, the author emphasizes short, clear descriptions which are implemented by references to authoritative manuscripts. It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design, and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise. This book is intended for anyone who is involved in ASIC design implementation -- starting from physical design to final design signoff. Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design.

Physical Design Essentials - Khosrow Golshan 2007-04-08

Arranged in a format that follows the industry-common ASIC physical design flow, Physical Design Essentials begins with general concepts of an ASIC library, then examines floorplanning, placement, routing, verification, and finally, testing. Among the topics covered are Basic standard cell design, transistor-sizing, and layout styles; Linear, non-linear, and polynomial characterization; Physical design constraints and floorplanning styles; Algorithms used for placement; Clock Tree Synthesis; Parasitic extraction; Electronic Testing, and many more.

Low Power Methodology Manual - David Flynn 2007-07-31

This book provides a practical guide for engineers doing low power System-on-Chip (SoC) designs. It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches. In addition to providing a theoretical basis for these techniques, the book addresses the practical issues of implementing them in today's designs with today's tools.

VLSI Physical Design: From Graph Partitioning to Timing Closure - Andrew B. Kahng 2011-01-27

Design and optimization of integrated circuits are essential to the creation of new semiconductor chips, and physical optimizations are becoming more prominent as a result of semiconductor scaling. Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor technologies and increased problem complexities. A user of such software needs a high-level understanding of the underlying mathematical models and algorithms. On the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance bottlenecks and how various algorithms operate and interact. "VLSI Physical Design: From Graph Partitioning to Timing Closure" introduces and compares algorithms that are used during the physical design phase of integrated-circuit design, wherein a geometric chip layout is produced starting from an abstract circuit design. The emphasis is on essential and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.

Static Timing Analysis for Nanometer Designs - J. Bhasker 2009-04-03

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

Design and Modeling of Low Power VLSI Systems - Sharma, Manoj 2016-06-06

Very Large Scale Integration (VLSI) Systems refer to the latest development in computer microchips which are created by integrating hundreds of thousands of transistors into one chip. Emerging research in this area has the potential to uncover further applications for VSLI technologies in addition to system advancements. Design and Modeling of Low Power VLSI Systems analyzes various traditional and modern low power techniques for integrated circuit design in addition to the limiting factors of existing techniques and methods for optimization. Through a research-based discussion of the technicalities involved in the VLSI hardware development process cycle, this book is a useful resource for researchers, engineers, and graduate-level students in computer science and engineering.

High-Performance and Time-Predictable Embedded Computing - Pinho, Luis Miguel 2018-07-04

Nowadays, the prevalence of computing systems in our lives is so ubiquitous that we live in a cyber-physical world dominated by computer systems, from pacemakers to cars and airplanes. These systems demand for more computational performance to process large amounts of data from multiple data sources with guaranteed processing times. Actuating outside of the required timing bounds may cause the failure of the system, being vital for systems like planes, cars, business monitoring, e-trading, etc. High-Performance and Time-Predictable Embedded Computing presents recent advances in software architecture and tools to support such complex systems, enabling the design of embedded computing devices which are able to deliver high-performance whilst guaranteeing the application required timing bounds. Technical topics discussed in the book include: Parallel embedded platformsProgramming modelsMapping and scheduling of parallel computationsTiming and schedulability analysisRuntimes and operating systems The work reflected in this book was done in the scope of the European project P-SOCRATES, funded under the FP7 framework program of the European Commission. High-performance and time-predictable embedded computing is ideal for personnel in computer/communication/embedded industries as well as academic staff and master/research students in computer science, embedded systems, cyber-physical systems and internet-of-things.

Constraining Designs for Synthesis and Timing Analysis - Sridhar Gangadharan 2014-07-08

This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

Flip-Flop Design in Nanometer CMOS - Massimo Alioto 2014-10-14

This book provides a unified treatment of Flip-Flop design and selection in nanometer CMOS VLSI systems. The design aspects related to the energy-delay tradeoff in Flip-Flops are discussed, including their energy-optimal selection according to the targeted application, and the detailed circuit design in nanometer CMOS VLSI systems. Design strategies are derived in a coherent framework that includes explicitly nanometer effects, including leakage, layout parasitics and process/voltage/temperature variations, as main advances over the existing body of work in the field. The related design tradeoffs are explored in a wide range of applications and the related energy-performance targets. A wide range of existing and recently proposed Flip-Flop topologies are discussed. Theoretical foundations are provided to set the stage for the derivation of design guidelines, and emphasis is given on practical aspects and consequences of the presented results. Analytical models and derivations are introduced when needed to gain an insight into the inter-dependence of design parameters under practical constraints. This book serves as a valuable reference for practicing engineers working in the VLSI design area, and as text book for senior undergraduate, graduate and postgraduate students (already familiar with digital circuits and timing).

Lunar Sourcebook - Grant Heiken 1991-04-26

The only work to date to collect data gathered during the American and Soviet missions in an accessible

and complete reference of current scientific and technical information about the Moon.

Nanometer Technology Designs - Nisar Ahmed 2010-02-26

Traditional at-speed test methods cannot guarantee high quality test results as they face many new challenges. Supply noise effects on chip performance, high test pattern volume, small delay defect test pattern generation, high cost of test implementation and application, and utilizing low-cost testers are among these challenges. This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test.

Static Timing Analysis for Nanometer Designs - J. Bhasker 2009-04-17

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

Timing Optimization Through Clock Skew Scheduling - Ivan S. Kourtev 2012-12-06

History of the Book The last three decades have witnessed an explosive development in integrated circuit fabrication technologies. The complexities of cur rent CMOS circuits are reaching beyond the 100 nanometer feature size and multi-hundred million transistors per integrated circuit. To fully exploit this technological potential, circuit designers use sophisticated Computer-Aided Design (CAD) tools. While supporting the talents of innumerable microelectronics engineers, these CAD tools have become the enabling factor responsible for the successful design and implemen tation of thousands of high performance, large scale integrated circuits. This research monograph originated from a body of doctoral disserta tion research completed by the first author at the University of Rochester from 1994 to 1999 while under the supervision of Prof. Eby G. Friedman. This research focuses on issues in the design of the clock distribution net work in large scale, high performance digital synchronous circuits and particularly, on algorithms for non-zero clock skew scheduling. During the development of this research, it has become clear that incorporating timing issues into the successful integrated circuit design process is of fundamental importance, particularly in that advanced theoretical de velopments in this area have been slow to reach the designers' desktops.

IBM Power E1080 Technical Overview and Introduction - Scott Vetter 2022-11-01

This IBM® Redpaper® publication provides a broad understanding of a new architecture of the IBM Power® E1080 (also known as the Power E1080) server that supports IBM AIX®, IBM i, and selected distributions of Linux operating systems. The objective of this paper is to introduce the Power E1080, the most powerful and scalable server of the IBM Power portfolio, and its offerings and relevant functions: Designed to support up to four system nodes and up to 240 IBM Power10TM processor cores The Power E1080 can be initially ordered with a single system node or two system nodes configuration, which provides up to 60 Power10 processor cores with a single node configuration or up to 120 Power10 processor cores with a two system nodes configuration. More support for a three or four system nodes configuration is to be added on December 10, 2021, which provides support for up to 240 Power10 processor cores with a full combined four system nodes server. Designed to supports up to 64 TB memory The Power E1080 can be initially ordered with the total memory RAM capacity up to 8 TB. More support is to be added on December 10, 2021 to support up to 64 TB in a full combined four system nodes server. Designed to support up to 32 Peripheral Component Interconnect® (PCIe) Gen 5 slots in a full combined four system nodes server and up to 192 PCIe Gen 3 slots with expansion I/O drawers The Power E1080 supports initially a maximum of two system nodes; therefore, up to 16 PCIe Gen 5 slots, and up to 96 PCIe Gen 3 slots with expansion I/O drawer. More support is to be added on December 10, 2021, to support up to 192 PCIe Gen 3 slots with expansion I/O drawers. Up to over 4,000 directly attached serial-attached SCSI (SAS) disks or solid-state drives (SSDs) Up to 1,000 virtual machines (VMs) with logical partitions (LPARs) per system System control unit, providing redundant system master Flexible Service Processor (FSP) Supports IBM Power System Private Cloud Solution with Dynamic Capacity This publication is for professionals who want to acquire a better understanding of Power servers. The intended audience includes the following roles: Customers Sales and marketing professionals Technical support professionals IBM Business Partners Independent software vendors (ISVs) This paper does not replace the current marketing materials and configuration tools. It is intended as an extra source of information that, together with existing sources, can be used to enhance your knowledge of IBM server solutions.

An ASIC Low Power Primer - Rakesh Chadha 2012-12-05

This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices. Readers will benefit from the hands-on approach which starts form the ground-up, explaining with basic examples what power is, how it is measured and how it impacts on the design process of application-specific integrated circuits (ASICs). The authors use both the Unified Power Format (UPF) and Common Power Format (CPF) to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent. From analyzing system power consumption, to techniques that can be employed in a low power design, to a detailed description of two alternate standards for capturing the power directives at various phases of the design, this book is filled with information that will give ASIC designers a competitive edge in low-power design.

Verilog Hdl Synthesis, a Practical Primer - J. Bhasker 2018-05-21

With this book, you can: - Start writing synthesizable Verilog models quickly. - See what constructs are supported for synthesis and how these map to hardware so that you can get the desired logic. - Learn techniques to help avoid having functional mismatches. - Immediately start using many of the models for commonly used hardware elements described for your own use or modify these for your own application.

Thermal and Rheological Measurement Techniques for Nanomaterials Characterization - Sabu Thomas 2017-05-23

Thermal and Rheological Measurement Techniques for Nanomaterials Characterization, Second Edition covers thermal and rheological measurement techniques, including their principle working methods, sample preparation and interpretation of results. This important reference is an ideal source for materials scientists and industrial engineers who are working with nanomaterials and need to know how to determine their properties and behaviors. Outlines key characterization techniques to determine the thermal and rheological behavior of different nanomaterials Explains how the thermal and rheological behavior of nanomaterials affect their usage Provides a method-orientated approach that explains how to successfully use each technique

Timing Performance of Nanometer Digital Circuits Under Process Variations - Victor Champac 2018-04-18

This book discusses the digital design of integrated circuits under process variations, with a focus on design-time solutions. The authors describe a step-by-step methodology, going from logic gates to logic paths to the circuit level. Topics are presented in comprehensively, without overwhelming use of analytical formulations. Emphasis is placed on providing digital designers with understanding of the sources of process variations, their impact on circuit performance and tools for improving their designs to comply with product specifications. Various circuit-level “design hints” are highlighted, so that readers can use then to improve their designs. A special treatment is devoted to unique design issues and the impact of process variations on the performance of FinFET based circuits. This book enables readers to make optimal decisions at design time, toward more efficient circuits, with better yield and higher reliability.

Visualizing Chemistry - National Research Council 2006-06-01

Scientists and engineers have long relied on the power of imaging techniques to help see objects invisible to the naked eye, and thus, to advance scientific knowledge. These experts are constantly pushing the limits of technology in pursuit of chemical imaging—the ability to visualize molecular structures and chemical

composition in time and space as actual events unfold—from the smallest dimension of a biological system to the widest expanse of a distant galaxy. Chemical imaging has a variety of applications for almost every facet of our daily lives, ranging from medical diagnosis and treatment to the study and design of material properties in new products. In addition to highlighting advances in chemical imaging that could have the greatest impact on critical problems in science and technology, Visualizing Chemistry reviews the current state of chemical imaging technology, identifies promising future developments and their applications, and suggests a research and educational agenda to enable breakthrough improvements.

The Design Warrior's Guide to FPGAs - Clive Maxfield 2004-06-16

Field Programmable Gate Arrays (FPGAs) are devices that provide a fast, low-cost way for embedded system designers to customize products and deliver new versions with upgraded features, because they can handle very complicated functions, and be reconfigured an infinite number of times. In addition to introducing the various architectural features available in the latest generation of FPGAs, The Design Warrior’s Guide to FPGAs also covers different design tools and flows. This book covers information ranging from schematic-driven entry, through traditional HDL/RTL-based simulation and logic synthesis, all the way up to the current state-of-the-art in pure C/C++ design capture and synthesis technology. Also discussed are specialist areas such as mixed hardward/software and DSP-based design flows, along with innovative new devices such as field programmable node arrays (FPNAs). Clive "Max" Maxfield is a bestselling author and engineer with a large following in the electronic design automation (EDA)and embedded systems industry. In this comprehensive book, he covers all the issues of interest to designers working with, or contemplating a move to, FPGAs in their product designs. While other books cover fragments of FPGA technology or applications this is the first to focus exclusively and comprehensively on FPGA use for embedded systems. First book to focus exclusively and comprehensively on FPGA use in embedded designs World-renowned best-selling author Will help engineers get familiar and succeed with this new technology by providing much-needed advice on choosing the right FPGA for any design project

A Practical Approach to VLSI System on Chip (SoC) Design - Veena S. Chakravarthi 2019-09-25

This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system on chip (SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF-based low power design flow issues for deep submicron SOC designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade, and will also be a valuable professional reference for those already working in VLSI design and verification with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers; Covers end-to-end VLSI SoC design flow; Includes source code, case studies, and application examples.

VLSI Interview Questions with Answers - Sam Sony 2012

If you can spare half an hour, then this ebook guarantees job search success with VLSI interview questions. Now you can ace all your interviews as you will access to the answers to the questions, which are most likely to be asked during VLSI interviews. You can do this completely risk free, as this book comes with 100% money back guarantee. To find out more details including what type of other questions book contains, please click on the BUY link.

Concurrency, Compositionality, and Correctness - Dennis Dams 2010-02-12

Why would you read this preface? As we start thinking what to write here, we wonder who is going to read these words. Fromourperspective–thatofwritersaddressinganaudienceofreaders–you are most likely Willem-Paul de Roever. Willem: our main motivation in putting together this Festschrift is to honor you on the occasion of your retirement. In terms of scienti?c ancestry, you are a father to two of us, and a grandfather to 1 the third , and you have had a profound impact on our formation as computer scientists.Atthepersonallevel,weknowyouasakind-hearted,generousperson. We are grateful to know you in these ways, and hope to have encounters with you in many years to come.

AnotherlikelypossibilityisthatyouareCorinneorJojanneke,wifeordau- ter of Willem; the two strong pillars on which so much in his life is founded. You share the honor,respect, and love that went into the writing, as will be ackno- edged by those contributing authors that know you – which are almost all. Also, we would like to thank you for your help in sending us photographs for inclusion in this book, and for your encouragement. The next option is that you are one of the contributing authors. In this case you may wonder why it took us so long to get this work published. After all, wasn’tit“almostdone”alreadyattheretirementeventinJuly2008?Theanswer is twofold: we gave everyone ample time to revise their submissions in line with the recommendations by the referees; and we ourselves took ample time to put everything together. Our hope is that this will be visible in the quality of the ?nal result.

Digital Logic Design Using Verilog - Vaibbhav Taraate 2016-05-17

This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

Static Timing Analysis for Nanometer Designs - J. Bhasker 2011-09-08

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

CMOS - R. Jacob Baker 2008

This edition provides an important contemporary view of a wide range of analog/digital circuit blocks, the BSIM model, data converter architectures, and more. The authors develop design techniques for both long- and short-channel CMOS technologies and then compare the two.

Feedback Systems - Karl Johan Åström 2021-02-02

The essential introduction to the principles and applications of feedback systems—now fully revised and expanded This textbook covers the mathematics needed to model, analyze, and design feedback systems. Now more user-friendly than ever, this revised and expanded edition of Feedback Systems is a one-volume resource for students and researchers in mathematics and engineering. It has applications across a range of disciplines that utilize feedback in physical, biological, information, and economic systems. Karl Åström and Richard Murray use techniques from physics, computer science, and operations research to introduce control-oriented modeling. They begin with state space tools for analysis and design, including stability of solutions, Lyapunov functions, reachability, state feedback observability, and estimators. The matrix exponential plays a central role in the analysis of linear control systems, allowing a concise development of many of the key concepts for this class of models. Åström and Murray then develop and explain tools in the frequency domain, including transfer functions, Nyquist analysis, PID control, frequency domain design, and robustness. Features a new chapter on design principles and tools, illustrating the types of problems that can be solved using feedback Includes a new chapter on fundamental limits and new material on the Routh-Hurwitz criterion and root locus plots Provides exercises at the end of every chapter Comes with an electronic solutions manual An ideal textbook for undergraduate and graduate students Indispensable for

researchers seeking a self-contained resource on control theory

Design, Automation, and Test in Europe - Rudy Lauwereins 2008-01-08

In 2007 The Design, Automation and Test in Europe (DATE) conference celebrated its tenth anniversary. As a tribute to the chip and system-level design and design technology community, this book presents a compilation of the three most influential papers of each year. This provides an excellent historical overview of the evolution of a domain that contributed substantially to the growth and competitiveness of the circuit electronics and systems industry.

Flow Cytometry and Cell Sorting - Andreas Radbruch 2013-06-29

The practical aspects of flow cytometry and sorting are emphasized in this book which introduces the beginner to the technology and provides tips and tricks for the advanced user. The clear structure makes it easy to address specific problems fast. The chapters cover the modern applications of these procedures, with emphasis on immunofluorescence (antibody-fluorochrome conjugation, staining principles and data evaluation); the isolation of specific chromosomes, cells and fragile, large particles by magnetic and fluorescence-activated sorting; cellular biochemistry; and the dynamics of proliferation. The methods have been field-tested in recent EMBO courses on flow cytometry.

Nanometer CMOS ICs - Harry J.M. Veendrick 2017-04-28

This textbook provides a comprehensive, fully-updated introduction to the essentials of nanometer CMOS integrated circuits. It includes aspects of scaling to even beyond 12nm CMOS technologies and designs. It clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design implementation and application. Coverage includes all associated disciplines of nanometer CMOS ICs, including physics, lithography, technology, design, memories, VLSI, power consumption, variability, reliability and signal integrity, testing, yield, failure analysis, packaging, scaling trends and road blocks. The text is based upon in-house Philips, NXP Semiconductors, Applied Materials, ASML, IMEC, ST-Ericsson, TSMC, etc., courseware, which, to date, has been completed by more than 4500 engineers working in a large variety of related disciplines: architecture, design, test, fabrication process, packaging, failure analysis and software.

EDA for IC Implementation, Circuit Design, and Process Technology - Luciano Lavagno 2018-10-03

Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit Design, and Process Technology, thoroughly examines real-time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.